AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancelled).

2. (Cancelled).

3. (Cancelled).

4. (Cancelled).

5. (Original) A graphics processor, including:

image processing circuitry; and

an embedded frame buffer;

wherein the embedded frame buffer is selectively configurable to received data in any of the following formats:

- point sampled color and depth;

- super-sampled color and depth; and

- YUV.

6. (Original) The graphics processor of claim 5, wherein the point sampled format is a 48-bit format and the super-sampled format is a 96-bit format.

7. (Original) The graphics processor of claim 6, wherein the 48-bit format includes 24 color bits and 24 depth bits.

8. (Original) The graphics processor of claim 7, wherein the embedded frame buffer is further configurable such that the 24 color bits selectively include either 8 bits

for red, 8 bits for blue and 8 bits for green (RGB8) or 6 bits for red, 6 bits for green, 6 bits for blue and 6 bits for alpha (RGBA6).

9. (Original) The graphics processor of claim 7, wherein the 96-bit format includes color and depth data for three super-sample locations for a pixel.

10. (Original) The graphics processor of claim 9, wherein the super-sample color data is 16 bits and the super-sample depth data is 16 bits.

11. (Original) The graphics processor of claim 10, wherein the 16 bit super-sample color data includes 5 bits for red, 6 bits for green and 5 bits for blue (R5G6B5).

12. (Original) The graphics processor of claim 5, wherein the YUV format is a YUV 4:2:0 format.

13. (Original) The graphics processor of claim 5, wherein the embedded frame buffer is a dynamic random access memory (DRAM).

14. (Original) A graphics system, comprising a graphics chip having graphics processing circuitry and an embedded frame buffer for storing frame data prior to sending the frame data to an external location, wherein the embedded frame buffer is selectively configurable between the following pixel formats:

- RGB8 and 24 bit Z;
- RGBA6 and 24 bit Z;
- Three R5G6B5 color and 16 bit Z super-samples; and
- YUV 4:2:0.

15. (Original) The graphics system of claim 14, wherein in the YUV 4:2:0 configuration, a color buffer of the embedded frame buffer is partitioned to store 720x576 Y, 360x288 U and 360x288 V image planes for a YUV 4:2:0 frame.

16. (Original) The graphics system of claim 15, wherein the color buffer partitioning allocates as follows:

- 1024x640 8 bit Y image;
- 528x320 8 bit U image; and
- 528x320 8 bit V image.

17. (Original) The graphics system of claim 14, further including an interface to the graphics system that enables a programmer to selectively configure the embedded frame buffer.

18. (Original) The graphics system of claim 17, wherein the interface enables the embedded frame buffer to be reconfigured on a frame-by-frame basis.

19. (Original) In a graphics chip having pixel processing circuitry and an embedded frame buffer for storing pixel data prior to transferring the pixel data to an external destination, an improvement comprising:

a reconfigurable embedded frame buffer which can be selectively configured to store any of the following pixel formats:

- 48 bit point sampled color and Z;
- 96 bit super-sampled color and Z; and
- YUV.

20. (Original) The graphics chip of claim 19, wherein the embedded frame buffer is further selectively configurable to store the following 48 bit formats:

- RGB8 and 24 bit Z; and
- RGBA6 and 24 bit Z.

21. (Original) The graphics chip of claim 19, wherein the 96 bit super-sampled format includes three super-samples each having a R5G6B5 color and 16 bit Z format.

22. (Original) The graphics chip of claim 19, wherein the YUV format is a YUV 4:2:0 format.

23. (Original) A method of using an embedded frame buffer in a graphics system, including the steps of:

providing an embedded frame buffer that is selectively configurable to store image data in either RGB color format or YUV color format; and

providing an interface to the graphics system which controls the configuration of the embedded frame buffer.

24. (Original) The method of claim 23, further including enabling the interface to selectively configure the embedded frame buffer on a frame-by-frame basis.

25. (Original) The method of claim 23, further including enabling the RGB color format to be configured as either a 48-bit point sampled color and Z format or a 96-bit super-sampled color and Z format.

26. (Original) The method of claim 25, further including enabling the 48-bit format to selectively include an RGB8 and 24 bit Z format or an RGBA6 and 24 bit Z format.

27. (Original) The method of claim 25, further including defining the 96-bit super-sample format to include three super-samples each having a R5G6B5 color and 16 bit Z format.

28. (Original) The method of claim 23, further including defining the YUV format as a YUV 4:2:0 format.